

# 4L-Q100ZR4-70

QSFP28 100GBASE-ZR4, 1310nm, SM, DDM, LC, 70Km



## Applications

- Compliant with 100GBASE-ER4 Ethernet
- 4 LAN-WDM lanes MUX/DEMUX design
- Up to 103.1 Gbps Bit Rate
- Datacenter backbones
- Maximum power consumption 6.5W
- 4 x 25GBASE Ethernet
- SAN, Routers, Hubs, Load Balancer
- High-performance Computing Clusters
- Other optical links

## Features

- QSFP28 100G Optical Transceiver
- QSFP28 MSA Compliant
- Up to 70Km links on SMF
- 3.3v power supply
- EML WDM TOSA laser transmitter
- ADP ROSA receiver
- Duplex LC receptacles
- 4x 25Gb/s LAN-WDM
- Digital Diagnostic Monitoring
- RoHS-6 and Lead Free
- Operating temperature: 0°C ~ +70°C

## Description

The 4L-Q100ZR4-70 is a QSFP28 four channel full duplex transceiver module for singlemode (SMF) 100GBASE-ZR4 / 100 Gigabit optical data communications.

This modules are compatible with most switch/router/server brands and designed to operate with single mode fiber (SMF) and Duplex LC connectors, using 4 channels of 25Gb/s LAN-WDM with up to 70km.

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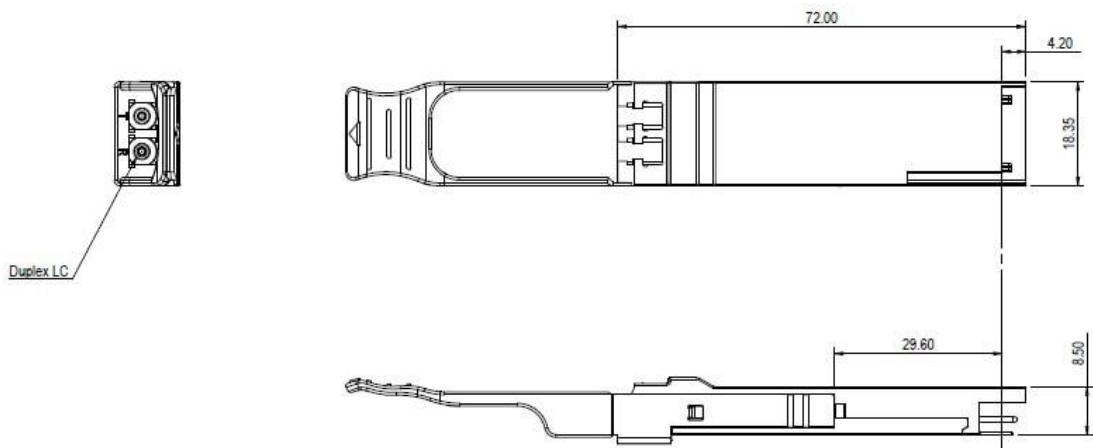
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## General Specifications – Recommended Ratings

Parameter	Symbol	Min	Typ	Max
Max Link Length	Lmax			70Km on SMF
Supply Voltage	Vcc	3.135v	3.3v	3.465v
Power Consumption				4.5W
Storage Temperature	T <sub>s</sub>	-40		85
Case Operating Temperature	T <sub>OP</sub>	0°C		70
Relative Humidity	RH	15		85
Receiver Damage Threshold, per Lane	pRdmg	3.4		
Bit Rate (all wavelngths)	BR			103.1Gb/s
Bit Error Ratio – pre FEC	BER			10 <sup>-12</sup>

## Mechanical Specifications



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## Optical Specifications - Transmitter

Parameter	Symbol	Min	Typical	Max	Unit
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm
	L1	1299.02	1300.05	1301.09	nm
	L2	1303.54	1304.58	1305.63	nm
	L3	1308.09	1309.14	1310.19	nm
<b>Transmitter</b>					
SMSR	SMSR	30			dB
Total Average Launch Power	p <sub>T</sub>	+8		+12.5	dBm
Average Launch Power, each Lane	p <sub>AVG</sub>	+2.0		+4.5	dBm
OMA, each Lane	p <sub>OMA</sub>	0.1		4.5	dBm
Difference in Launch Power	P <sub>tx,diff</sub>			3.6	dB
Launch Power in OMA		-0.5			dBm
TDP, each Lane	TDP			2.5	dB
Extinction Ratio	ER	6.0			dB
RIN <sub>20OMA</sub>	RIN			-130	dB/H
Optical Return Loss	TOL			20	dB
Transmitter Reflectance	r <sub>T</sub>			-12	dB
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3				{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}	
Average Launch Power OFF	P <sub>off</sub>			-30	dBm

## Optical Specifications – Receiver

Receiver				
Damage Threshold	THd	6.5		dBm
Average Receive Power		-22	-4.5	dBm
Receive Power (OMA)			-1.9	dBm
Receiver Sensitivity (OMA), each Lane (BER = $5 \times 10^{-5}$ )	SEN1		-21.5	dBm
Receiver Sensitivity (OMA), each Lane (BER = $1 \times 10^{-12}$ )	SEN2		-25.5	dBm
Stressed Receiver Sensitivity (OMA), each Lane (BER = $5 \times 10^{-5}$ )	SEN3		-14	dBm
Receiver Sensitivity (OMA), each Lane (BER = $5 \times 10^{-5}$ )	SEN4		-16	dBm
Receiver Sensitivity (OMA), each Lane (BER = $1 \times 10^{-12}$ )	SEN5		-13	dBm
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff		3.6	dB
LOS Assert	LOSA	-38		dBm
LOS Deassert	LOSD		-29	dBm
LOS Hysteresis	LOSH	0.5		dB
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc		31	GHz

## Electrical Specifications

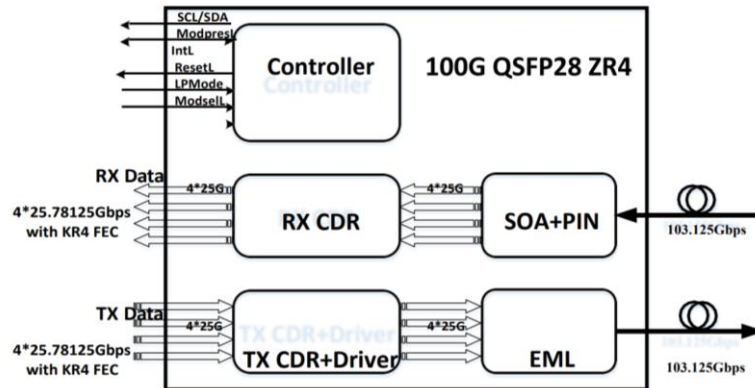
Parameter	Symbol	Min	Typical	Max
Power Consumption	P			4.5 W
Supply Current	I <sub>cc</sub>			1.360 A
Transceiver Power-on Initialization Time				2000 ms
<b>Transmitter</b>				
Single-ended Input Voltage Tolerance		-350mV		2850mV
AC Common Mode Input Voltage Tolerance		15 mV		
Differential Input Voltage		50 mVpp		
Differential Input Voltage Swing	V <sub>in</sub>			900 mVpp
Differential Input Impedance	Z <sub>in</sub>	90	100	110 Ohm
<b>Receiver</b>				
Single-ended Output Voltage		-0.3		4.5 W
AC Common Mode Output Voltage				7.5 mV
Differential Output Voltage Swing	V <sub>out</sub>	300		850 mVpp
Differential Output Impedance	Z <sub>out</sub>	90	100	110 Ohm

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## Transceiver Block Diagram



**ModSelL** : The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and deasserting periods of different modules may overlap as long as the above timing requirements are met.

**ResetL** : The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length ( $t_{Reset\_init}$ ) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time ( $t_{init}$ ) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset ( $t_{init}$ ) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data\_Not\_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

**LPMODE**: The LPMODE pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMODE pin and a combination of the Power override, Power\_set and High\_Power\_Class\_Enable software control bits (Address A0h, byte 93 bits 0,1,2). ModPrsL: ModPrsL is pulled up to Vcc\_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

**IntL**: IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636)

## Pin Description

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Non-Inverted Data Output	
25	Rx4p	Receiver Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	
30	VccI	+3.3V Power supply	
31	LPMODE	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

### Notes

1. Circuit ground is internally isolated from chassis ground.

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## Ordering Information

Part Number	Description
4L-Q100SR4-M100	QSFP28 100GBASE-SR4, 850nm, MM, DDM, MPO/MTP, 100m
4L-Q100BSR4-100	QSFP28 100GBASE-SR4, 850/900nm, BiDi MM, DDM, LC, 150m
4L-Q100CW4-02	QSFP28 100GBASE-CWDM4, LC, DDM, SM 2km.
4L-Q100PLR4-M02	QSFP28 100GBASE-PLR4, 1310nm, SM, DDM, MPO/MTP, 2km
4L-Q100LR4-10	QSFP28 100GBASE-LR4, 1310nm, SM, DDM, Duplex LC, 10Km
4L-Q100LR4-20	QSFP28 100GBASE-LR4, 1310nm, SM, DDM, Duplex LC, 20Km
4L-Q100ER4-40	QSFP28 100GGBASE-ER4, 1310nm, SM, DDM, Duplex LC, 40Km
4L-Q100ZR4-70	QSFP28 100GGBASE-ZR4, 1310nm, SM, DDM, Duplex LC, 70Km
4L-Q100ZR4-80	QSFP28 100GGBASE-ZR4, 1310nm, SM, DDM, Duplex LC, 80Km

### Note

This modules have been tested by 4LAN on equipment like Cisco, Juniper, Dell, HP, Mikrotik, Huawei, and other brands. The equipment brand must be informed before shipping the order, so the transceivers are reprogrammed to the corresponding brand.

### Contact Information

Website: [www.4-lan.com](http://www.4-lan.com)

Email: [contato@brazilmkt.com.br](mailto:contato@brazilmkt.com.br)

Telephone: +55 11 5521-2522

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